AMENDMENTS TO THE CLAIMS

1. (Currently amended) A method for testing a plurality of content addressable memory (CAM) cells in a CAM device, comprising the steps of:

(a) testing said CAM device to identify stuck match lines by conducting a 1-pattern or 0-pattern search match line test ~~to a given match line~~ and repairing or disabling row addresses for the CAM device which corresponds to rows having stuck match lines;

(b) testing said CAM device to identify defective pull down lines using a walking 1 or 0 match pattern ~~across the identified stuck match lines~~ and repairing or disabling cells at bit positions identified as having defective pull down lines;

(c) testing each CAM cell in said CAM device to locate a faulty CAM cell ~~within said defective pull down lines~~; and

(d) for each located faulty CAM cell identified in step (c), diagnosing a cause of fault for said faulty CAM cell by applying at least one signal to said faulty CAM cell and reading a state of the match line associated with said faulty cell.

2. (Currently amended) The method of claim 1, wherein step (c) is performed after both steps (a) and (b)~~, and step (d) is performed after step (c)~~.

3. (Original) The method of claim 1, wherein said step of applying at least one signal comprises:

setting a mask value of said faulty CAM cell to a logical zero; and

identifying a faulty match line if said match line is set to logical zero.

4. (Original) The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a search data line of said faulty CAM cell to a logical one;

setting a complement search data line of said faulty CAM cell to a logical zero; and

identifying a faulty match line if said match line is set to logical zero.

5. (Original) The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complement search data line of said faulty CAM cell to a logical one; and

identifying a faulty match line if said match line is set to logical zero.

6. (Original) The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complement search data line of said faulty CAM cell to a logical one; and

identifying a faulty match line if said match line is set to logical one.

7. (Original) The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical one;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying a faulty search data line if said match line is set to logical one.

8. (Original) The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical one;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a faulty search data line if said match line is set to logical zero.

9. (Original) The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a faulty complement search data line if said match line is set to a logical one.

10. (Original) The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying a faulty complement search data line if said match line is set to logical zero.

11. (Original) The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical one;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying an stuck open fault with a transistor having a gate coupled to a data storage node of said CAM cell, if said match line is set to logical one.

12. (Original) The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying an short circuit fault with a transistor having a gate coupled to a data storage node of said CAM cell, if said match line is set to logical zero.

13. (Original) The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying an stuck open fault with a transistor having a gate coupled to a complement of a data storage node if said match line is set to a logical one.

14. (Original) The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical one;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to is set to a logical one; and

identifying a short circuit fault with a transistor having a gate coupled to a complement of a data storage node, if said match line is set to logical zero.

15. (Original) The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a stuck open fault with a transistor having a gate coupled to a search data line, if said match line is set to logical one.

16. (Previously presented) The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying a short circuit fault with a transistor having a gate coupled to a search data line, if said match line is set to logical one.

17. (Original) The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a stuck open fault with a transistor having a gate coupled to a complementary search data line, if said match line is set to one.

18. (Original) The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying a short circuit fault with a transistor having a gate coupled to a complementary search data line, if said match line is set to logical zero.

19. (Original) The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical one;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one; and

setting a complementary search data line of said faulty CAM cell to a logical zero;

identifying a stuck open fault with a transistor having a gate coupled to a mask register, if said match line is set to logical one.

20. (Original) The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a stuck open fault with a transistor having a gate coupled to a mask register, if said match line is set to logical one.

21. (Previously presented) The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical one;

setting a mask value of said faulty CAM cell to a logical zero;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying a short circuit fault with a transistor having a gate coupled to a mask register, if said match line is set to logical zero.

22. (Original) The method of claim 1, wherein said step of applying at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical zero;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a short circuit fault with a transistor having a gate coupled to a mask register, if said match line is set to logical zero.

23. (Previously presented) A system for testing a CAM device comprising:

an interface for sending and receiving signals from the CAM device; and

a processor, coupled to said interface, for controlling signals that are sent to the CAM device and for reading signals received from the CAM device,

wherein said processor operates said interface to test said CAM device for stuck match lines by conducting a 1-pattern search or 0-pattern search match line test ~~to a given match line~~, repairing or disabling row addresses for the CAM device which correspond to rows having stuck match lines; to test said CAM device for defective pull down lines using a walking 1 or 0 match pattern ~~across the stuck match lines~~, repairing or disabling cells at bit positions identified as having defective pull down lines; and to test each CAM cell to locate faulty CAM cells; and

wherein for each faulty CAM cell said processor operates said interface to diagnose a cause of fault for each faulty CAM cell by applying at least one signal and reading a state of a match line associated with the faulty CAM cell.

24. (Previously presented) The system of claim 23, wherein said processor applies said at least one signal comprises:

setting a mask value of said faulty CAM cell to a logical zero; and

identifying a faulty match line if said match line is set to logical zero.

25. (Previously presented) The system of claim 23, wherein said processor applies said at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a search data line of said faulty CAM cell to a logical one;

setting a complement search data line of said faulty CAM cell to a logical zero; and

identifying a faulty match line if said match line is set to logical zero.

26. (Previously presented) The system of claim 23, wherein said processor applies said at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complement search data line of said faulty CAM cell to a logical one; and

identifying a faulty match line if said match line is set to a logical zero.

27. (Previously presented) The system of claim 23, wherein said processor applies said at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complement search data line of said faulty CAM cell to a logical one; and

identifying a faulty match line if said match line is set to logical one.

28. (Previously presented) The system of claim 23, wherein said processor applies said at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical one;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying a faulty search data line if said match line is set to logical one.

29. (Previously presented) The system of claim 23, wherein said processor applies said at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical one;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a faulty search data line if said match line is set to logical zero.

30. (Previously presented) The system of claim 23, wherein said processor applies said at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a faulty complement search data line if said match line is set to a logical one.

31. (Previously presented) The system of claim 23, wherein said processor applies said at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying a faulty complement search data line if said match line is set to logical zero.

32. (Previously presented) The system of claim 23, wherein said processor applies said at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical one;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying an stuck open fault with a transistor having a gate coupled to a data storage node of said CAM cell, if said match line is set to logical one.

33. (Previously presented) The system of claim 23, wherein said processor applies said at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying an short circuit fault with a transistor having a gate coupled to a data storage node of said CAM cell, if said match line is set to logical zero.

34. (Previously presented) The system of claim 23, wherein said processor applies said at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying an stuck open fault with a transistor having a gate coupled to a complement of a data storage node if said match line is set to a logical one.

35. (Previously presented) The system of claim 23, wherein said processor applies said at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical one;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to is set to a logical one; and

identifying a short circuit fault with a transistor having a gate coupled to a complement of a data storage node, if said match line is set to logical zero.

36. (Previously presented) The system of claim 23, wherein said processor applies said at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a stuck open fault with a transistor having a gate coupled to a search data line, if said match line is set to logical one.

37. (Previously presented) The system of claim 23, wherein said processor applies said at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying a short circuit fault with a transistor having a gate coupled to a search data line, if said match line is set to logical one.

38. (Previously presented) The system of claim 23, wherein said processor applies said at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a stuck open fault with a transistor having a gate coupled to a complementary search data line, if said match line is set to one.

39. (Previously presented) The system of claim 23, wherein said processor applies said at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying a short circuit fault with a transistor having a gate coupled to a complementary search data line, if said match line is set to logical zero.

40. (Previously presented) The system of claim 23, wherein said processor applies said at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical one;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying a stuck open fault with a transistor having a gate coupled to a mask register, if said match line is set to logical one.

41. (Previously presented) The system of claim 23, wherein said processor applies said at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical one;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a stuck open fault with a transistor having a gate coupled to a mask register, if said match line is set to logical one.

42. (Previously presented) The system of claim 23, wherein said processor applies said at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical one;

setting a mask value of said faulty CAM cell to a logical zero;

setting a search data line of said faulty CAM cell to a logical one;

setting a complementary search data line of said faulty CAM cell to a logical zero; and

identifying a short circuit fault with a transistor having a gate coupled to a mask register, if said match line is set to logical zero.

43. (Previously presented) The system of claim 23, wherein said processor applies said at least one signal comprises:

setting a storage location of said faulty CAM cell to a logical zero;

setting a mask value of said faulty CAM cell to a logical zero;

setting a search data line of said faulty CAM cell to a logical zero;

setting a complementary search data line of said faulty CAM cell to a logical one; and

identifying a short circuit fault with a transistor having a gate coupled to a mask register, if said match line is set to logical zero.

44. (Previously presented) A system for testing a CAM device comprising:

means for testing for stuck match line within the device by conducting a 1-pattern or 0-pattern search match line test ~~to a given match line~~ and repairing or disabling row addresses for the CAM device which corresponds to rows having stuck match lines;

means for testing for defective pull down lines within the device using a walking 1 or 0 match pattern ~~across the identified stuck match lines~~ and repairing or disabling cells at bit positions identified as having defective pull down lines;

means for identifying faulty CAM cells within the device; and

means for diagnosing faulty CAM cells identified by said identifying means.